

AP20 Rec'd PCT/PTO 30 MAY 2006

**Description****INTERLEAVING METHOD FOR LOW DENSITY  
PARITY CHECK ENCODING****Technical Field**

- [1] The present invention relates to an interleaving method, and more particularly, to an interleaving method for achieving a high error correction rate when burst errors are generated in an encoding process using a low density parity check (LDPC) matrix.

**Background Art**

- [2] A low density parity check (LDPC) encoding and decoding method refers to an error correction encoding and decoding technology used in a wireless communication field and an optical recording/reproducing field. The LDPC encoding method was initially suggested by Gallager in 1962. However, since it was very difficult to manufacture a decoder at that time, the LDPC encoding method has been abandoned. Recently, the LDPC method is repropose by Mackey.
- [3] The LDPC encoding method includes a process of generating parity information using a parity check matrix. Here, most components of the parity check matrix are 0, and very sparse components of the parity check matrix are 1. The LDPC encoding method has an excellent error correction performance by performing repeatedly an encoding process using an adding/multiplying algorithm. For example, an irregular LDPC encoding process where the length of encoding language is  $10^6$  and an encoding rate is 1/2 has a performance closer to the Shannon limit, better than that of a turbo encoding process.
- [4] The LDPC encoding process is divided into a regular LDPC encoding process and an irregular LDPC encoding process. In the regular LDPC encoding process, the number of components of '1' included in a parity check matrix used for encoding and decoding is the same in every row and in every column. Otherwise, the LDPC encoding process is irregular. In the regular LDPC encoding process, the numbers of 1s included in each row and each column are called a row weight and a column weight, respectively.
- [5] The LDPC encoding process can be represented as shown in Equation 1.
- [6] [Equation 1]
- [7]  $H \times C = 0$
- [8] Here, H indicates a parity check matrix, 0 indicates a zero matrix, '×' indicates an XOR operation and a modular 2 operation, and C indicates a code word vector, that is,

a column matrix indicating a code word to be encoded. The code word includes an  $x$ -bit message word  $x_1, x_2, \dots, x_x$  and  $p$ -bit parity information  $p_1, p_2, \dots, p_p$ .

[9] The parity information  $p_1, p_2, \dots, p_p$  is generated so that the message word  $x_1, x_2, \dots, x_x$  satisfies Equation 1. That is, since a binary value of the message word to be coded among components of the parity check matrix  $H$  and matrix  $C$  is determined, parity information  $p_i$  ( $i=1, 2, \dots, p$ ) can be determined using Equation 1.

[10] A more detailed description of the LDPC encoding process is described in 'Good Error Correction Codes Based on Very Sparse Matrices' (D.J. MacKay, IEEE Trans. on Information Theory, vol. 45, no.2, pp.399-431, 1999).

[11] Interleaving technologies deal with burst errors. In a communication or storage medium system, when a signal passes through a channel, a burst error on a specific portion of the transmitted signal can be generated. The burst error is generated by an external cause of a transmission medium in the communication system and by a scratch of a storage medium in the storage medium system. Since the burst error is generated on a specific location of a transmitted bit stream, if information existing on the specific location has been dispersed on other positions and is relocated on the original location when a decoding process is performed in a receiving end, an error volume of the location where the burst error is generated can be reduced. The residual error can be restored using information of a zone where an error is not generated, for example, parity information.

[12] The interleaving technologies can also be applied to the LDPC encoding process. One of the interleaving technologies applied to the LDPC is to generate error correction blocks using a plurality of code word vectors generated by a parity check matrix, divide the error correction blocks into predetermined sized unit blocks, and interleave the unit blocks. However, when a conventional interleaving method is applied as it is, no information exists with respect to the size of interleaving unit for interleaving more effectively. That is, when a conventional interleaving method is applied to an LDPC encoding process, the size of an interleaving unit effective for the burst error correction of the LDPC encoding process is unknown.

## **Disclosure of Invention**

### **Technical Solution**

[13] The present invention provides an interleaving method of increasing reliability of error correction by determining the size of an optimum interleaving unit when a low density parity check (LDPC) encoding process is performed.

### **Advantageous Effects**

- [14] According to the present invention, provided is an interleaving method of increasing reliability of error correction by determining the size of an optimum interleaving unit when an LDPC encoding process is performed.

### **Description of Drawings**

- [15] FIG. 1 is a schematic diagram of an encoding process and decoding process in a communication and storage medium system;
- [16] FIG. 2 illustrates a correlation between a parity check matrix and a generated code word vector in a low density parity check (LDPC) encoding process;
- [17] FIG. 3 illustrates a correlation between a location of 1 in an LDPC encoded code word vector and the size of a burst error;
- [18] FIG. 4 illustrates code word vectors each having a different interleaving unit size;
- [19] FIG. 5 illustrates a conventional method of determining the size of an interleaving unit when an error correction limit is 1 bit;
- [20] FIG. 6 illustrates a case where a code word vector is changed when interleaving and de-interleaving processes are performed by applying an interleaving unit according to an embodiment of the present invention; and
- [21] FIG. 7 illustrates a correlation between the reliability of error correction and the size of an interleaving unit when an error correction limit is 1 bit.

### **Best Mode**

- [22] According to an aspect of the present invention, there is provided an interleaving method used for a low density parity check (LDPC) encoding process, the method comprising: generating more than one code word vector by generating parity information on the basis of a parity check matrix; dividing the generated code word vector into interleaving units, each having the size determined on the basis of bit lengths between 1s included in a row of the parity check matrix; and interleaving the more than one code word vector using the interleaving unit.
- [23] The dividing of the generated code word vectors into interleaving units comprises: extracting a maximum range bit length including only the 1s with respect to all 1s included in the row of the parity check matrix; and determining the size of interleaving unit on the basis of the extracted bit lengths.
- [24] According to another aspect of the present invention, there is provided a method of determining the size of interleaving unit in an LDPC encoding process, the method comprising: extracting code word bits corresponding to components equal to 1 in a row of a parity check matrix in a code word vector as valid code word bits; extracting

bit lengths between the valid code word bits in the code word vector; and determining the size of an interleaving unit on the basis of the bit lengths between the valid code word bits.

### Mode for Invention

- [25] Hereinafter, the present invention will now be described more fully with reference to the accompanying drawings, in which embodiments of the invention are shown.
- [26] FIG. 1 is a schematic diagram of an encoding process and decoding process in a communication and storage medium system.
- [27] An LDPC encoder 110 receives an original message word 111 to be transmitted and generates a plurality of code word vectors 121 by LDPC encoding the original message word 111. Each code word vector 121 includes the message word 111 and parity information generated to satisfy Equation 1 described above. An interleaver 120 receives the plurality of code word vectors 121 and generates an interleaved bit stream 131 by building an error correction block, dividing the error correction block into pre-determined size of interleaving units, and dispersing the interleaving units on suitable locations. In a communication system, the interleaved bit stream 131 is transmitted via a transmission medium such as air, and in a storage medium system, the interleaved bit stream 131 is transferred to a reproducing apparatus as it was recorded on a storage medium.
- [28] In a receiving end or a reproducing apparatus, a de-interleaver 130 receives the interleaved bit stream 131 and generates the code word vectors 141 by de-interleaving the interleaved bit stream 131. An LDPC decoder 140 receives the code word vectors 141 and generates the original message word 142 using an LDPC decoding algorithm.
- [29] FIG. 2 illustrates a correlation between a parity check matrix and a generated code word vector in an LDPC encoding process.
- [30] An LDPC encoding process is a process of generating parity information in a code word vector  $A$  so that a result of an XOR operation and a modular operation of a parity check matrix  $H$  and the code word vector  $A$  is a zero matrix. To know the parity information  $p_1, p_2, \dots$  existing in one code word vector, as many functions as the number of rows of the parity check matrix  $H$  are generated. The LDPC encoding process is a process of obtaining the parity information  $p_1, p_2, \dots$  by solving the functions. In the embodiment of FIG. 2, since the number of rows of the parity check matrix  $H$  is 10, 10 functions are generated.
- [31] Since the 10 functions are generated by the XOR and modular operations of the rows of the parity check matrix  $H$  and the code word vector  $A$ , only 1s in the rows of

the parity check matrix  $H$  influence the generation of the functions. Therefore, only 1s included in each row  $R_1, R_2, \dots$  of the parity check matrix  $H$  influence the encoding process, and components equal to 0 included in each row  $R_1, R_2, \dots$  of the parity check matrix  $H$  do not influence a result of the encoding process.

[32] In FIG. 2, shaded components 201, 202, and 203 in a row  $R_1$  of the parity check matrix  $H$  indicates the 1s, and shaded components 211, 212, and 213 in the code word vector  $A$  indicate components XOR and modular operated with the components 201, 202, and 203 of the parity check matrix  $H$ . In other words, the other components (non-shaded components in the code word vector  $A$  of FIG. 2) except the components 211, 212, and 213 in the code word vector  $A$  do not influence the LDPC encoding process.

[33] An LDPC decoding algorithm is a process of generating the original code word vector  $A$  from a received code word vector  $A'$ . All currently used decoding algorithms use Equation 1 used for the encoding process. That is, a decoding process is performed on the basis of locations of '1s' existing in rows of a parity check matrix. This means that the code word bits 211, 212, and 213 corresponding to these locations in the code word vector  $A$  are decoded using the same decoding algorithm in the decoding process.

[34] An interleaving process is a process of dividing all code word vectors  $A, B, C, \dots$  into predetermined sized interleaving units and placing the interleaving units on different locations according to a predetermined rule. In the interleaving process, determining the size of interleaving unit much influences reliability of error correction when a burst error is generated.

[35] If the code word vectors are transmitted through transmission channel or recorded on a storage medium using a maximum interleaving unit, that is, sequentially without the interleaving process, since all code word bits placed on a location where a burst error is generated belong to the same code word vector, a problem that a specific code word vector cannot be decoded is generated. Also, if the size of interleaving unit is too small, a complex problem is generated when de-interleaving and it is not easy to realize the small sized interleaving unit due to a limit according to the size of error correction block. Therefore, it is important for achieving the high reliability of error correction to determine the optimum size of interleaving unit.

[36] FIG. 3 illustrates a correlation between a location of 1 in an LDPC encoded code word vector and the size of a burst error.

[37] In FIG. 3, shaded code word bits, which are the code word bits 211, 212, and 213

corresponding to locations, in which components of the parity check matrix are '1', in the code word vector of FIG. 2, are defined as valid code word bits. If a burst error E1 is generated, code word bits distorted by the burst error E1 are a third bit through a seventh bit. The code word bits distorted by the burst error E1 include one valid code word bit. If a burst error E2 is generated, code word bits distorted by the burst error E2 are a second bit through a eighth bit. That is, the code word bits distorted by the burst error E2 include two valid code word bit.

- [38] The size of interleaving unit is related to the number of valid code word bits influenced by a buster error in a code word vector. This will be described in detail with reference to FIGS. 4 and 5.
- [39] FIG. 4 illustrates code word vectors each having a different interleaving unit size. FIG. 4 shows a correlation between the size of interleaving unit and the number of valid code word bits in a code word vector.
- [40] A first case of FIG. 4 shows that the interleaving unit is 5bits, and a second case shows that the interleaving unit is 7bits. An interleaving process is not performed yet. When interleaving units BI1, BI2, ... are transmitted via a channel or recorded on a storage medium, since each interleaving unit BI1, BI2, ... is placed on a different l ocaton, that is, since the interleaving units BI1, BI2, ... are interleaved, the in-terleaving units BI1, BI2, ... are not influenced by the same burst error. Therefore, even if a burst error larger than the interleaving unit is generated, only an interleaving unit having bits as many as a maximum size is influenced by the burst error in a code word vector. Also, it is assumed that an error correction limit is 1 bit.
- [41] In the first case, the interleaving unit BI1 includes one valid code word bit. It is assumed that a burst error is generated on a location where the interleaving unit BI1 is placed and the size of burst error is 8 bits. Even if the size of burst error is 8 bits, since the interleaving units are influenced by the burst error after they are interleaved, the burst error influencing the interleaving unit BI1 cannot influence a de-interleaved in-terleaving unit BI2.
- [42] As described in FIG. 3, since only valid code word bits influence parity in-formation in a code word vector when the LDPC encoding process is performed, and since the number of valid code word bits included in the interleaving unit BI1 is 1, the error generated on the code word vector A is a 1-bit error. Since the interleaving unit BI2 is not located nearby the interleaving unit BI 1 anymore in the channel or medium by interleaving process, the error does not influence the interleaving unit BI2 although the size of burst error is 8 bit. The error can be corrected.

- [43] In the second case, an interleaving unit BF1 includes two valid code word bits. Like the first case, it is assumed that a burst error is generated on a location where the interleaving unit BF1 is placed and the size of burst error is 8 bits as shown in FIG. 4. Unlike the first case, since the number of valid code word bits included in the interleaving unit BF1 is 2, the error generated on the code word vector A is a 2-bit error. The error cannot be corrected.
- [44] In FIG. 4, arrow marks indicate zones influenced by the same burst error with respect to the two interleaving units. Even if an 8-bit burst error is generated in the two cases, since the interleaving unit is 5 bits in the first case, only the 5 bits were influenced by the burst error, and since the interleaving unit is 7 bits in the second case, the 7 bits were influenced by the burst error. The residual 3 bits influenced by the burst error of the first case and the residual 1 bit influenced by the burst error of the second case will be placed in any one of code word vectors B, C, .... Since the code word bits influenced by the burst error, which are placed in any one of code word vectors B, C, ..., belong to different code word vectors, the code word bits are not related to the error correction of the code word vector.
- [45] In sum, the size of the interleaving unit must be determined so that each interleaving unit has valid code word bits within the error correction limit. In the embodiment of FIG. 4, since it is assumed that the error correction limit is 1 bit, each interleaving unit must have one or no valid code word bit.
- [46] FIG. 5 illustrates a conventional method of determining the size of an interleaving unit when an error correction limit is 1 bit.
- [47] In FIG. 5, horizontally arranged round dots indicate code word bits in a specific code word vector. Also, shaded round dots correspond to valid code word bits,  $n$  indicates a length of the specific code word vector,  $M$  indicates an average length between valid code word bits, and  $L$  indicates a maximum number of bits including only one valid code word bit.
- [48] As described above, to correct a burst error, interleaving units must be determined so that each interleaving unit has valid code word bits within the error correction limit. Accordingly, a maximum value of the size of interleaving unit permitted in FIG. 5 is  $L$ . The  $L$  value is different for every code word vector, and also different according to how many valid code word bits the range of the  $L$  value includes even in one code word vector.
- [49] However, if the average length  $M$  between valid code word bits can be measured, a value of the maximum length  $L$  including only one valid code word bit should be

double the M value. Therefore, the maximum size of an interleaving unit BImax and the M value are in the following relationship:

[50] [Equation 2]

[51]  $B_{\text{Imax}} = L \cdot 2M$

[52] Here, BImax indicates the maximum size of interleaving unit, L indicates a maximum length of bits including only one valid code word bit, and M indicates an average length between valid code word bits.

[53] Here, the reason why the L value is not the same as the 2M value is because lengths between valid code word bits are different according to code word vectors and different for every code word bits even in the same code word vector. That is, lengths between 1s in a parity check matrix are different even if they are in the same row.

[54] In particular, in the regular LDPC encoding process, the number of valid code word bits included in a code word vector is the same as a row weight Wr of a parity check matrix. Also, an average length between valid code word bits is the same as a value divided the length of code word vector n by the row weight Wr of the parity check matrix. Therefore, in the regular LDPC encoding process, the maximum value of the size of interleaving unit BImax can be represented as shown in Equation 3.

[55] [Equation 3]

[56]  $B_{\text{Imax}} = L \cdot 2M = 2n/W_r$

[57] Here, n indicates a length of a code word vector, and Wr indicates a row weight of a parity check matrix.

[58] If the error correction limit is 2 bits not 1 bit,  $L = 3M$ , and if the error correction limit is 3 bits,  $L = 4M$ , ..., and if the error correction limit is k bits,  $L = (k+1)M$ . Accordingly, Equation 3 is generalized as shown in Equation 4.

[59] [Equation 4]

[60]  $B_{\text{Imax}} = L = (k+1)M = (k+1)n/W_r$

[61] Here, k indicates an error correction limit, n indicates a length of a code word vector, and Wr indicates a row weight.

[62] FIG. 6 illustrates a case where a code word vector is changed when interleaving and de-interleaving processes are performed by applying an interleaving unit according to an embodiment of the present invention.

[63] A first drawing shows a bit stream including code word vectors A, B, C, ... before they are interleaved. The non-interleaved code word vectors A, B, C, ... include interleaving units A1, A2, A3, ..., B1, B2, B3, ..., C1, C2, C3, ..., respectively.

[64] A second drawing shows a bit stream after the interleaving units A1, A2, A3, ...,



B1, B2, B3, ..., C1, C2, C3, ... are interleaved using a predetermined method. The used interleaving method interleaves the bit stream by alternatively extracting interleaving units of code word vectors. The interleaved bit stream is transmitted via a communication channel or stored in a storage medium.

- [65] A third drawing shows a bit stream after the bit stream is de-interleaved in a receiving end or a reproducing apparatus. Here, it is assumed that a burst error is generated on a location where A2, B2, and C2 are placed. The burst error distorted the interleaving units A2, B2, and C2 to interleaving units EA2, EB2, EC2. The distorted interleaving units EA2, EB2, EC2 is replaced in the original code word vectors by a de-interleaving process.
- [66] A fourth drawing shows an internal configuration of a code word vector A after de-interleaving. Here, the interleaving unit EA2 includes one valid code word bit. Therefore, the interleaving unit EA2 can be corrected by the other non-distorted interleaving units A1, A3, A4, .... If the size of interleaving unit is determined so that each interleaving unit includes two or more valid code word bits, since the interleaving unit EA2 includes two or more valid code word bits, the de-interleaved code word vector A includes two or more valid code word bits. As a result, the error cannot be corrected.
- [67] FIG. 7 illustrates a correlation between the reliability of error correction and the size of an interleaving unit when an error correction limit is 1 bit.
- [68] As described above, according to the spirit of the present invention, a maximum value, which an interleaving unit can have in a regular LDPC encoding process, is  $2n/W_r$ . Therefore, a possible range of an interleaving unit BI is  $1 < BI < 2n/W_r$ . The larger the n value, and the less the  $W_r$  value, the more the maximum value of the interleaving unit BI increases. FIG. 7 shows that the reliability of error correction dramatically drops near  $2n/W_r$ .
- [69] That the reliability of error correction decreases at values smaller than the  $2n/W_r$  value is because a bit length between 1s is not fixed in a parity check matrix. That is, since bit lengths between valid code word bits are not constant in all code word vectors or the same code word vector, a valid code word bit length having a value smaller than  $n/W_r$  assumed as the average value can exist. Therefore, the reliability of error correction can increase a little more by determining a little smaller value than  $2n/W_r$  as the interleaving unit size. Here, a difference D between the  $2n/W_r$  value and the size of optimum interleaving unit  $BI_{opt}$  decreases as a distribution uniformity of 1s included in a parity check matrix is higher and as a density of 1s is lower, that is, as a row weight

is smaller.

[70] The present invention provides a method of optimally selecting the size of an interleaving unit. To do this, the best is to extract all  $L$  values and determine a smaller size than any  $L$  value as the size of the interleaving unit. However, it is also possible to regard a  $2M$  value as the  $L$  value and determine a smaller value than the  $2M$  value as the size of the interleaving unit. More simply, a smaller value than a  $2n/W_r$  value can be regarded as the size of the interleaving unit. In the last two cases, even though the reliability of error correction decreases compared with the first case, the reliability increases compared with the conventional method that does not account for a bit length between valid code word bits.

[71] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The preferred embodiments should be considered in descriptive sense only and not for purposes of limitation. Therefore, the scope of the invention is defined not by the detailed description of the invention but by the appended claims, and all differences within the scope will be construed as being included in the present invention.